DE-EMBEDDING DEVICES UNDER TEST

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates in general to electronic circuits and in particular to de-embedding devices.

Description of the Related Art

[0002] In the design of integrated circuits such as e.g. high-frequency / RF integrated circuits, it is desired that only the intrinsic characteristics of the underlying semiconductor devices be incorporated in the design process. Typically, determination of the intrinsic characteristics is accomplished in a manner such that unwanted parasitics are introduced into the characterization process, due to the process of fabricating the associated test devices. De-embedding is a process that is utilized to remove the effects of the parasitics from the characteristics of a device under test.

[0003] Figures 1-4 are functional schematics of 2-port test structures typically used in prior art de-embedding processes. Figure 1 is a schematic representation of test structure 101 that includes a transmission configured two terminal device under test (DUT) 111, shown as a two-port network. Examples of such devices include capacitors, diodes, inductors, resisters, or any other two terminal device. In one embodiment, DUT 111 is fabricated on a substrate of a semiconductor wafer with input port 103 and output port 107 located on the wafer surface for radio frequency (rf) characterization.

[0004] Figure 2 is a schematic representation of a "thru" test structure typically used for de-embedding the electrical characteristics of DUT 111. It is desirable that test structure 201 have the same electrical length and port characteristics as test structure 101 exclusive of DUT 111.

[0005] Figure 3 is a schematic representation of a "short" test structure typically used for de-embedding the electrical characteristics of DUT 111. It is desirable that test structure 301 have the same port characteristics and the same electrical length as test structure 101, but with rf "shorts" at locations corresponding to the locations of port-1 and port-2 of DUT111.

[0006] Figure 4 is a schematic representation of an "open" test structure typically used for de-embedding the electrical characteristics of DUT 111. It is desirable that test structure 401 have the same port characteristics and the same electrical length as test structure 101, but with rf "opens" at locations corresponding to the locations of port-1 and port-2 of DUT111.

[0007] Test structures 201, 301, and 401 are constructed from the same fabrication process as test structure 101 of Figure 1.

[0008] A prior art process of de-embedding typically involves the collection of scattering (S) parameters on test structures 101, 201, 301, and 401. The S parameters from test structure 101 are then modified to remove the effects of parasitics associated with test structure 101 as determined from the S parameters collected from test structures 201, 301, and 401. With some prior art de-embedding processes, test structure 201 may not be required.

[0009] The process of de-embedding described above requires the fabrication of three additional test structures (201, 301, and 401). Each additional test structure requires/occupies additional wafer area and increases testing time and complexity. What is desired is an improved process of de-embedding.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0011] Figure 1 is a schematic representation of a test structure used in a prior art de-embedding process.

[0012] Figure 2 is a schematic representation of a test structure used in a prior art de-embedding process.

[0013] Figure 3 is a schematic representation of a test structure used in a prior art de-embedding process.

[0014] Figure 4 is a schematic representation of a test structure used in a prior art de-embedding process.

[0015] Figure 5 is a schematic representation of a test structure used in one embodiment of a de-embedding process according to the present invention.

[0016] Figure 6 is a schematic representation of a test structure used in one embodiment of a de-embedding process according to the present invention.

[0017] Figure 7 is a flow diagram setting forth one embodiment of a de-embedding process according to the present invention.

[0018] Figure 8 is a schematic representation illustrating one embodiment of a partitioning of the electrical characteristics of a thru test structure into electrical characteristics of two two-port networks according to the present invention.

[0019] Figure 9 shows one embodiment of equations setting forth constraints in partitioning the electrical characteristics of a thru test structure into electrical characteristics of two two-port networks according to the present invention.

[0020] Figure 10 sets forth one embodiment of an equation for obtaining intrinsic characteristics of a device under test according to the present invention.

[0021] Figure 11 is a flow diagram setting forth one embodiment of a method for design and fabricating an integrated circuit according to the present invention.

[0022] Figure 12 is block diagram of one embodiment of a system for obtaining intrinsic characteristics of a DUT according to the present invention.

[0023] The use of the same reference symbols in different drawings indicates identical items unless otherwise noted.

DETAILED DESCRIPTION

[0024] The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

[0025] Figure 5 is a schematic representation of test structure 501 that includes a transmission configured two terminal device under test (DUT) 511. DUT 511 is a device in which it is desired to obtain its intrinsic properties. Examples of such devices include

capacitors, diodes, inductors, resisters, or any other two terminal device in an integrated circuit. Circuit 513 represents the parasitics of the structures between input port 503 and DUT 511, and circuit 515 represents the parasitics of the structures between output port 507 and DUT 511.

[0026] In one embodiment, DUT 511 is fabricated on the substrate of a semiconductor wafer with input port 503 and output port 507 located on the wafer surface for radio frequency (rf) characterization. In one embodiment, ports 503 and 507 are implemented in a ground-signal-ground (GSG) configuration. However, structure 501 may represent test structures having other testing configurations.

[0027] Figure 6 is a schematic representation of a thru test structure 601, exclusive of the DUT, used for de-embedding the electrical characteristics of DUT 511. In one embodiment, test structure 601 is fabricated from the same process as test structure 501 of Figure 5. Circuit 613 represents the parasitics associated with input port 603 and circuit 615 represents the parasitics associated with the output port 607 of thru test structure 601. In one embodiment, test structure 601 has the same electrical length and port characteristics as test structure 501, exclusive of DUT 511.

[0028] Figure 7 is a flow diagram of setting forth one embodiment of a de-embedding process for obtaining intrinsic characteristics of a DUT. The de-embedding process shown in Figure 7 involves collecting sets of S parameters from two structures, test structure 501 and thru test structure 601.

[0029] In operation 703, S parameters are collected from DUT test structure 501. Referring back to Figure 5, in one embodiment of operation 703, the input reflection coefficient (S_{11} DUT), the output reflection coefficient (S_{22} DUT), the forward transmission coefficient (S_{21} DUT), and the reverse transmission coefficient (S_{12} DUT) are obtained from structure 501. In one embodiment, these parameters are obtained by rf characterizations of test structure 501 using a calibrated automatic network analyzer (ANA). See Figure 12.

[0030] In operation 705, S parameters are collected from thru test structure 601. Referring back to Figure 6, in one embodiment of operation 705, the input reflection coefficient (S_{11} THRU), the output reflection coefficient (S_{22} THRU), the forward transmission coefficient (S_{21} THRU), and the reverse transmission coefficient (S_{12} THRU)

are obtained from structure 601. In one embodiment, these parameters are obtained by rf characterizations of test structure 601 using a calibrated automatic network analyzer (ANA).

[0031] In operation 707, the electrical characteristics of thru test structure 601 (as represented by the S parameters obtained from thru test structure 601) are partioned into two sets of 2-port S parameters, an input set and an output set. Each set represents the characteristics of a two-port network.

[0032] Figure 8 represents characteristics of the equivalently partitioned thru network 801. Network 801 includes a two-port input network 809, a two-port output network 811, and a virtual reflectionless node 815. The S parameters of input network 809 and output network 811 are parameters that are partitioned from the S parameters obtained from thru test structure 601. The characteristics of network 809 and network 811 are such that when combined, result in the retention of the electrical characteristics of the thru test structure 601.

[0033] Virtual node 815 represents a reflectionless node representative of the point of insertion of a DUT.

[0034] Figure 9 sets forth the conditions for partitioning the electrical characteristics of thru test structure 601 into the S parameters associated with input network 809 and S parameters associated with output network 811. Regarding equation, 901, the input reflection coefficient (S_{11} IN) of input network 809 is set equal to the measured input reflection coefficient (S_{11} THRU) of test structure 601. Regarding equation, 903, the output reflection coefficient (S_{22} OUT) of output network 811 is set equal to the measured output reflection coefficient (S_{22} THRU) of test structure 601.

[0035] Regarding equation 905, the output refection coefficient (S_{22} IN) of input network 809 and the input reflection coefficient (S_{11} OUT) of the output network 811 are set such that a zero reflection coefficient (0 + j0) results.

[0036] Equations 907, 909, 911, 913 establish the transmission characteristics of input network 809 and output network 811. S_{21} IN is the forward transmission coefficient and S_{12} IN is the reverse transmission of input network 809. S_{21} OUT is the forward transmission coefficient and S_{12} OUT is the reverse transmission coefficient of output network 811. As shown in equations 907 and 911, the magnitude of the forward and reverse transmission coefficients of input network 809 and output network 811 are equal to the magnitude of the

forward and reverse transmission coefficients, respectively, obtained from thru test structure 601 raised to a power of 1 over a partitioning factor(X). As shown by equations 909 and 913, the angles of the forward and reverse transmission coefficients of input network 809 and output network 811 are equal to the angles of the forward and reverse transmission coefficients (S_{21} THRU and S_{12} THRU) respectively, divided by the partitioning factor.

[0037] X represents the a partitioning factor that, in one embodiment, is based on the geometric location of DUT 511 in the test structure 501. Referring back to Figure 5, in one embodiment, X is calculated as the distance from input port 503 to output port 507 (a+b) divided by the distance from DUT 511 to input port 503 (a). In embodiments where a is equal to b, the X partitioning factor is 2.

[0038] In one embodiment where the measured S parameters exist in real and imaginary format, the parameters are converted to magnitude and phase format for implementation of equations 907, 909, 911, and 913. Afterwards, the resultant S parameters are converted back to a real and imaginary format.

[0039] Referring back to Figure 7, in operation 709 the S parameters obtained from DUT test structure 601 and the partitioned characteristics of in network 809 and out network 811 are then converted to transmission (ABCD) parameters using standard conversion format.

[0040] In 711, the intrinsic characteristics of DUT 511 are derived (represented in ABCD parameters) using equation 1001 of Figure 10. $DMBD_{ABCD}$ represents a matrix of the intrinsic characteristics of DUT 511 in ABCD parameters. IN_{ABCD}^{-1} represents the inverse matrix of input network 809 characteristics in ABCD parameters. OUT_{ABCD}^{-1} represents the inverse matrix of output network 811 characteristics in ABCD parameters. As shown in equation 1001, the intrinsic characteristics of DUT 511 is derived by cascading the inverse matrix of the input network characteristics IN_{ABCD}^{-1} with the matrix of measured characteristics obtained from structure 501, and then cascading the resultant matrix with the inverse matrix of the output network characteristics OUT_{ABCD}^{-1}.

[0041] Referring back to Figure 7, the DUT characteristics (in ABCD parameters) are converted back to S parameters in 713.

[0042] Utilizing the above de-embedding process may provide a de-embedding process from which the intrinsic characteristics of a transmission configured two terminal device can

be derived from collecting data from only one additional test structure. Accordingly, such a de-embedding scheme may be implemented using less wafer space, require less testing time, and affording the ability to determine the desired characteristics directly via measurement.

[0043] Figure 11 is a flow diagram for fabricating an integrated circuit using the intrinsic characteristics obtained by a process similar to the process set forth in Figure 9. In 1103, the intrinsic characteristics of devices under test that were obtained from a de-embedding processes similar to that set forth in Figure 7 are incorporated in a design library. In 1105, the design library is used to produce a design for a circuit. In 1107, the circuit is fabricated from the design produced in 1105.

[0044] Figure 12 is block diagram of one embodiment of a system for obtaining intrinsic characteristics of a DUT according to the present invention. A DUT is located in a test structure 1205 fabricated on the substrate of wafer 1203. A thru test structure 1204 is also located on wafer 1203. Probes 1206 and 1207 are used to facilitate obtaining S parameter data from structure 1204 and structure 1205. The probes are operably coupled to calibrated automatic network analyzer 1209 (ANA). Network analyzer 1209 is controlled by code 1217 running on workstation 1211. Code 1217 is down loaded from storage media of 1217 (e.g. hard drives) of a server 1215 by workstation 1211. In other embodiments, code 1217 may be located on a hardrive of personal computer system or down loaded from a removable media (e.g. CDRom). In other embodiments, code 1217 may be executed by a processor located in network analyzer 1209. In one embodiment, the code is implemented in IC-CAP circuit simulation software sold by AGILENT-EESOF.

[0045] Set forth below is one embodiment of software code used for implementing operations 707, 709, 711, and 713 of Figure 7. The code is written in an adaptation of the BASIC language. This code is subject to copyright protection. The copyright owner has no objection to the facsimile reproduction by anyone of the patent document or the patent disclosure, as it appears in the Patent and Trademark Office patent file or records, but otherwise reserves all copyrights whatsoever.

[0046] Below is listed one embodiment of code for partitioning the measured S parameters of a thru test structure (e.g. 601) into a set of S parameters representative of an input network (e.g. 809).

```
i1=0
 i=0
 WHILE i < SIZE(thru)
   In_2_port.11[i]=thru.11[i1]
   !
   !********* S12 *********
   !
   Rev_Mag.12[i]=(real(thru.12[i1])^2+imag(thru.12[i1])^2)^0.5
   Mag_In_2_port.12[i]=Rev_Mag.12[i]^var2
   !
   Rev_Arg.12[i]=imag(thru.12[i1])//real(thru.12[i1])
   Angle_In_2_port.12[i]=atn(Rev_Arg.12[i])//var1
   !
   ! if Angle_In_2_port.12[i] > 0 then
   !    Angle_In_2_port.12[i] = Angle_In_2_port.12[i]-1.57
   ! end if
   !

Real_In_2_port.12[i]=cos(pct_1*Angle_In_2_port.12[i])*Mag_In_2
_port.12[i]

Imag_In_2_port.12[i]=sin(pct_1*Angle_In_2_port.12[i])*Mag_In_2
_port.12[i]
   !

In_2_port.12[i]=(Real_In_2_port.12[i])+j*(Imag_In_2_port.12[i]
)
   !
   !********* S21 *********
   !
   Fwd_Mag.21[i]=(real(thru.21[i1])^2+imag(thru.21[i1])^2)^0.5
   Mag_In_2_port.21[i]=Fwd_Mag.21[i]^var2
   !
   Fwd_Arg.21[i]=imag(thru.21[i1])//real(thru.21[i1])
   Angle_In_2_port.21[i]=atn(Fwd_Arg.21[i])//var1
   !
   ! if Angle_In_2_port.21[i] > 0 then
   !    Angle_In_2_port.21[i] = Angle_In_2_port.21[i]-1.57
   ! end if
   !

Real_In_2_port.21[i]=cos(pct_1*Angle_In_2_port.21[i])*Mag_In_2
_port.21[i]

Imag_In_2_port.21[i]=sin(pct_1*Angle_In_2_port.21[i])*Mag_In_2
_port.21[i]
   !

In_2_port.21[i]=(Real_In_2_port.21[i])+j*(Imag_In_2_port.21[i]
)
   !
```

```
   In_2_port.22[i]=0+j0
   i1=i1+1
   IF i1>=size_thru THEN i1=0
   i = i + 1
 END WHILE
 !
 RETURN In_2_port
```

[0047] Below is listed one embodiment of code for partitioning the S parameters of a thru test structure (e.g. 601) into a set of S parameters representative of an output network (e.g. 811).

```
i1=0
 i=0
 WHILE i < SIZE(thru)
   Out_2_port.11[i]=0+j0
   !
   !********* S12 ***********
   !
   Rev_Mag.12[i]=(real(thru.12[i1])^2+imag(thru.12[i1])^2)^0.5
   Mag_Out_2_port.12[i]=(Rev_Mag.12[i])^var2
   !
   Rev_Arg.12[i]=imag(thru.12[i1])//real(thru.12[i1])
   Angle_Out_2_port.12[i]=atn(Rev_Arg.12[i])//var1
   !
   ! if Angle_Out_2_port.12[i] > 0 then
   !    Angle_Out_2_port.12[i] = Angle_Out_2_port.12[i]-1.57
   ! end if
   !

Real_Out_2_port.12[i]=cos(pct_1*Angle_Out_2_port.12[i])*Mag_Ou
t_2_port.12[i]

Imag_Out_2_port.12[i]=sin(pct_1*Angle_Out_2_port.12[i])*Mag_Ou
t_2_port.12[i]
   !

Out_2_port.12[i]=(Real_Out_2_port.12[i])+j*(Imag_Out_2_port.12
[i])
   !
   !********* S21 ***********
   !
   Fwd_Mag.21[i]=(real(thru.21[i1])^2+imag(thru.21[i1])^2)^0.5
   Mag_Out_2_port.21[i]=(Fwd_Mag.21[i])^var2
   !
   Fwd_Arg.21[i]=imag(thru.21[i1])//real(thru.21[i1])
   Angle_Out_2_port.21[i]=atn(Fwd_Arg.21[i])//var1
   !
```

```
   ! if Angle_Out_2_port.21[i] > 0 then
   !    Angle_Out_2_port.21[i] = Angle_Out_2_port.21[i]-1.57
   ! end if
   !

Real_Out_2_port.21[i]=cos(pct_1*Angle_Out_2_port.21[i])*Mag_Ou
t_2_port.21[i]

Imag_Out_2_port.21[i]=sin(pct_1*Angle_Out_2_port.21[i])*Mag_Ou
t_2_port.21[i]
   !

Out_2_port.21[i]=(Real_Out_2_port.21[i])+j*(Imag_Out_2_port.21
[i])
   !
   Out_2_port.22[i]=thru.22[i1]
   i1=i1+1
   IF i1>=size_thru THEN i1=0
   i = i + 1
 END WHILE
 !
 RETURN Out_2_port
```

[0048] Below is one embodiment of code for converting a set of measured DUT test structure S parameters and sets of S parameters representative of an input network and an output network to sets of ABCD parameters. The code below also obtains the intrinsic characteristics of the DUT in ABCD parameters and converts them back to S parameters.

```
i1=0
 i=0
 WHILE i < SIZE(total)
   L_dummy_act.11[i]=L_dummy.11[i1]
   L_dummy_act.12[i]=L_dummy.12[i1]
   L_dummy_act.21[i]=L_dummy.21[i1]
   L_dummy_act.22[i]=L_dummy.22[i1]
   R_dummy_act.11[i]=R_dummy.11[i1]
   R_dummy_act.12[i]=R_dummy.12[i1]
   R_dummy_act.21[i]=R_dummy.21[i1]
   R_dummy_act.22[i]=R_dummy.22[i1]
   i1=i1+1
   IF i1>=size_dummy THEN i1=0
   i = i + 1
 END WHILE
 !
 PRINT "now do the de-embedding using ABCD matrix manipulation
..."
 !
 xtor=TwoPort(L_dummy_act,"S","A")^-1 * TwoPort(total,"S","A")
* TwoPort(R_dummy_act,"S","A")^-1
```

```
xtor=TwoPort(xtor,"A","S")
!
RETURN xtor
```

[0049] While particular embodiments of the present invention have been shown and described, it will be recognized to those skilled in the art that, based upon the teachings herein, further changes and modifications may be made without departing from this invention and its broader aspects, and thus, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention.